A Low Cost DSP Modem for HF Digital Experimentation[1]

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INTRODUCTION

This article describes an HF modulator-demodulator (modem) that is based on Digital Signal Processing (DSP) principles. A practical approach is shown, rather than the usual terse mathematics that usually accompanies this kind of discussion. This article is intended for those interested in experimenting with HF digital communications using DSP software. A low cost DSP platform is also described for implementing some of the ideas presented in this article including complete source code for a high performance HF digital modem.

What is DSP? To some, this means the manipulation of digital data to extract something meaningful. To the communications engineer, it actually means quite a bit more. Consider the following analogy: As experimenters, many are familiar with analog circuits that uses various interconnected components, such as resistors, capacitors, and operational amplifiers. The constructor uses some schematic or rather, an electrical behavioral model as a reference. Similarly, DSP in the most general sense, is the modellina of such systems in an all--digital domain, This involves sampling of real time signals where its accuracy, resolution, sample rate, as well as a multitude of algorithms plays an important role.

DEMODULATOR DESIGN

With that brief introduction, a little digression is necessary on the background of demodulation, in particular FSK (frequency shift keying) as used on the HF bands. It will become evident later, that this overview is appropriate for both analog and DSP demodulators.

After some experimentation with different types of demodulators, an experimenter soon realizes that the type of demodulator intended for use on HF is generally different than that used on telephone circuits, or that used on VHF. The main reason lies in the nature of the HF propagation. Not only has an HF demodulator have to deal with QRM, QRN, but also fading (QSB), multipath propagation, as well as with a very congested part of the RF

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spectrum. To design a well-engineered HF demodulator, one must pay special attention to several key factors such as dynamic range, i.e. the ability to work with both very weak and/or very strong signals, Superior selectivity is also required to deal with adverse signal to noise (S/N) conditions.

The area of HF demodulator design has evolved over the years to an almost, universal arrangement. This becomes evident when analyzing the modems of current TNC's (terminal node controllers). This typical arrangement, or architecture, is shown in Figure 1.

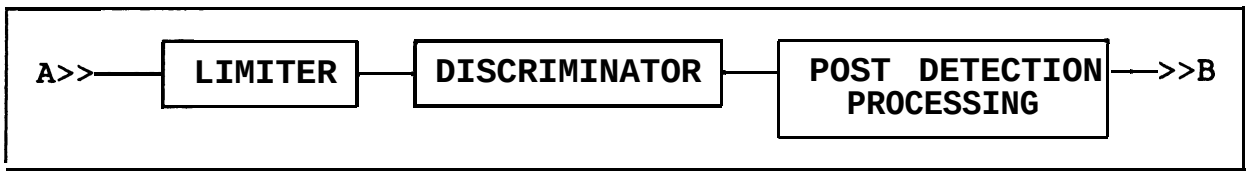


Figure 1. Conventional modem architecture. Audio input is at (A) and digital signal output is at (B).

The discriminator in these conventional designs, typically consists of a pair of filters, one each tuned to the mark and space tones respectively. The envelope of the outputs of the filters are extracted and combined as shown in Figure 2.

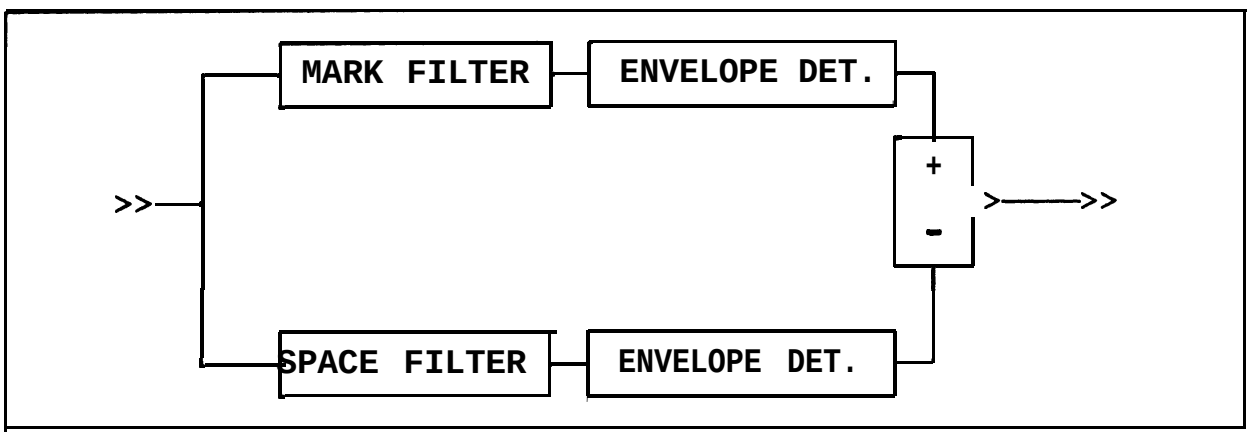


Figure 2. A conventional modem discriminator. Each filter is a bandpass filter centered at the appropriate tone frequency. The filter design loosely fits the specifications corresponding to a matched filter.

The operation of the demodulator is quite simple. The audio signal containing FSK tones is applied to the limiter at point (A) (please see Figure 1). The limiter produces a constant

amplitude, square-wave version of the input signal. One reason for this step is to remove amplitude variations on the FSK signal prior to detection. The function of the discriminator is to convert the input frequency to an analogous DC signal. It is obvious that, when, say a mark tone is present at the input, the mark discriminator filter will leave the mark signal unattenuated, but the space discriminator filter will attenuate the signal severely. The mark filter envelope detector will thus produce the equivalent of a positive envelope (a steady positive DC) and the space envelope detector will produce a near zero level, The combined output thus will be a positive DC level. Likewise if only a space tone is present, a negative DC level will be produced at the output of the discriminator. Such a discriminator will produce a classical **"S"** response when the frequency is swept between the mark and space tones where the upper part of the **"S"** corresponds to the positive part of the signal, i.e. the signal passing through the mark filter, while the lower part of the **"S"** corresponds to the signal passing through the space filter.

The remainder of the demodulator is concerned mainly with **post-** detection signal conditioning. I should be noted that, besides a DC level shift, the mark and space tone components, i.e. higher frequency components, are also present in the output of the discriminator. These tones are removed by a low **pass** filter. The remaining task of the demodulator is to threshold and convert the filtered DC levels to appropriate standard signal levels such as RS232 or TTL.

There are of course numerous variations on this basic theme, such as dealing with the efficiency of the various filters, balancing the outputs from the discriminator to track a small amounts of drift, or tolerate a limited amount of off-frequency operation.

In this discussion so far, the operation of the demodulator is nearly intuitively simple, however, this type of approach is what is known as a matched filter design, i.e. the detection of the tones is by means of filters that loosely matches the characteristic of the modulated tones. The reason why some demodulators perform better than others, even when the same architecture is used, lays fundamentally at the engineering principles of these matched filters. The theory of matched filters, is beyond the scope of this **article,** The **reader is** referred to the bibliography for further information.

Before we conclude this overview of demodulator architecture, several general, however, important observations must made. The first concerns signal phase. Note that any information regarding phase relationships within and between tones are of little consequence and plays no part in the detection process. When this is the case, the detection method is also known as noncoherent detection. One consequence of noncoherent detection is that it

requires somewhat more spectral bandwidth and also requires at least twice the shift magnitude than coherent detection. Its advantage is that its simple and cheap to implement.

The second observation deals with the usage of the limiter stage. This has been a controversy in the past. It was stated earlier that the purpose of the limiter was to remove any AM from the signal prior to detection. Its inclusion also has another purpose that has to do with non-linear characteristics introduced by the limiter. When a non-linear transformation of the input signal occurs, such as in the case of the limiter, the spectral content of the input signal is also modified. Theoretical research from the 1950's and 60's as well some practical evidence have shown that such a process perhaps may have desirable side-effects in signal capturing capability in the presence of strong competing signals (please see the bibliography for further references).

The third and final observation, also in context of the limiter stage, is dynamic range. Ideally, a demodulator should be able to cope with wide variations in signal levels such as often is the case when QSB is present or when dealing with weak signals. At one instance the signal level may be extremely low, then the next instant it may become very strong. When a limiter is used, its stage gain should be sufficient to handle all but the weakest of signals. Alternatively, as is used in this particular DSP modem, is to design a linear system with sufficient dynamic range so both weak and strong signals can be demodulated on an equal basis.

THE IMPLEMENTATION OF THE DSP DEMODULATOR

The DSP modem design that follows, employs several of the key components previously discussed in Figure 1, i.e. the matched filter detector and post detection processing. No limiter is used, however, special provision is made to increase dynamic range and provide additional improvement to the S/N ratio through a process of oversampling and decimation.

Most DSP applications involve analog to digital conversion (A/D) of the input signal. The rate at which the sampling and A/D takes place must be chosen rather carefully. As a minimum requirement, the sampling rate must be at least greater than twice the highest frequency present in the audio input. This is to prevent a phenomena called aliasing. The higher the rate the better, however, it must be kept in mind that the DSP must be able to complete its computational tasks associated with each sample before the next new sample can be processed. With first generation DSP's, this typically amounted to approximately 400 to 600 instructions for audio frequencies. If it is found that there is plenty of processing time to spare, a higher sampling rate may

be accommodated. This heavy demand on the amount of processing between input samples is one reason why general-purpose processors like the Intel 386/486 are not suited for DSP applications. Second generation fixed point DSP processors, like the TI 320C26 used in this DSP modem implementation, can quite easily accommodate even higher sample rates.

A further consideration concerning the choice of sample rate involves filter order. This factor may influence demodulator performance and usefulness. Larger filter orders at low sample rate generally mean **that** the signal lingers longer in the DSP and may thus introduce undesirable delays for timing-critical applications such as those in ARQ protocols.

Figure 3 presents the various components as employed in this DSP modem.

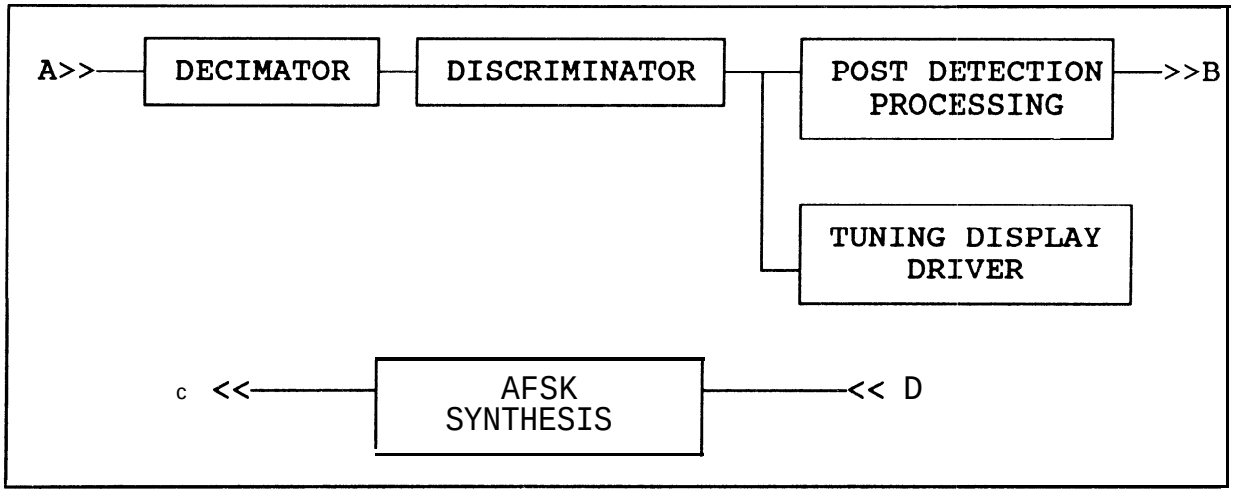


Figure 3. DSP modem architecture. The **analog** signal (A) is oversampled and decimated for increased dynamic range and better S/N. The discriminator consists of a pair of **matched** finite impulse response (FIR) filters. Post detection processing includes low pass filtering and thresholding for **data** output (B). A LED driver is provided for tuning purposes. Digital data for transmission is applied at (D) for digital audio frequency synthesis. This output, (C), is suitable for application to a SSB transceiver modulator.

DSP HARDWARE

Until fairly recently, DSP development tools, were very expensive and inaccessible to the average amateur experimenter. Recently, however, Texas Instruments (TI) released the TMS320C2x DSP starter Kit, also called the "DSK" (part number:TMDS3200026). For $99, the kit provides a small circuit module containing some DSP hardware, a thick user's guide, and a PC-based software package. All the user needs is a RS232 cable and 9V AC wall-mounted power transformer. This was intended as a low-cost introduction to DSP, and was received with great enthusiasm throughout the DSP community. The demand for the unit is so high that presently there is a world-wide shortage.

The software included a limited assembler, a nice debugger that executed the users' code on the DSP for real time debugging, and some coding examples to get you started. The DSP hardware module is a tiny circuit board measuring only 3.5 x 2.5 inches. All parts are surface-mounted which means that repairs would be very difficult. The DSP is a 40 MHz 320626 that has 1568 words on-chip static ram and a 256 word factory programmed ROM. At this clock rate, instructions typically execute in 100 ns. The on-chip RAM is configurable in several ways of code and data space configurations. The factory programmed ROM contains a simple bootstrap loader that allows the DSP memory to be loaded either from external memory, or via a RS232 line. The circuit module also contains a TLC32040 AIC that provides for a single channel, 14-bit A/D - D/A with sample rates as high as 44 kHz. The AIC is fully programmable and contains amongst-other things, programmable switched capacitor anti-aliasing and reconstruction filters.

Although the amount of RAM appears very limited, it actually goes a long way, in fact enough to implement our matched-filter HF demodulator and synthesized audio modulator.

DSP SOFTWARE

Sample Rate

As an example, software for a 2125 Hz mark, 2295 Hz space (170 Hz shift), 100 baud FSK demodulator will be shown. Specific details of the actual implementation of the demodulator should be read in conjunction with the source code. For availability of the DSP modem source code, please see the appendix.

The sample rate of matched filters for the DSP demodulator implementation is set at 6250 Hz. Since the space tone is set at 2295 Hz and the 100 baud modulation rate will extend the side

lobes of the spectrum to some extent. It thus appears that the chosen sample rate is adequate, (6250 > 2 x 2300 Hz).

Input Stage (decimator)

Consider the input decimator. The function of this stage, as previously discussed, is four fold:

a) Provide rejection of out-of-band signals, i.e. reject signals below 2125 Hz or above 2295.

b) Increase the dynamic range of the demodulator, i.e. for a 14-bit A/D the dynamic range is $20\log(1/(2^{14}-1)) = -84$ dB. It will be shown that the decimator used in this DSP demodulator behaves like a 21-element moving-average filter. The effect of such an arrangement is that each data value output is the result of a complex interpolation, i.e. each of the $2^{14}=16384$ quantized steps of the A/D convertor is further subdivided into much smaller steps. The actual dynamic range of such input stage will thus be in excess of 84 dB, which is quite impressive, however required for limiterless operation.

c) Increase the S/N ratio. If we assume that the input noise has a truly random behavior, the moving-average type input filter, will then by virtue of the additive nature of the signal component and noise components, cause the signal component to increase, while the noise component will tend to cancel. Unfortunately, some types of noise, such as static: crashes etc., does not behave in this way.

d) Reduce the sample rate for the matched-filter discriminator to.6250 Hz.

Decimators are actually rate downconvertors. They function by taking input samples, pushing them through a low-pass filter, and returns every N-th filter output for the result. The reason for the lowpass filter is to avoid new aliasing products being formed due to the lowered output sample rate. Since the matched-filter discriminator operates at 6250 Hz, the decimator is a x2 downconvertor and thus designed to operate at a sample rate of 12500 Hz. A special bandpass filter,, shown in Figure 4, is used with this decimator instead of the usual low pass filter,

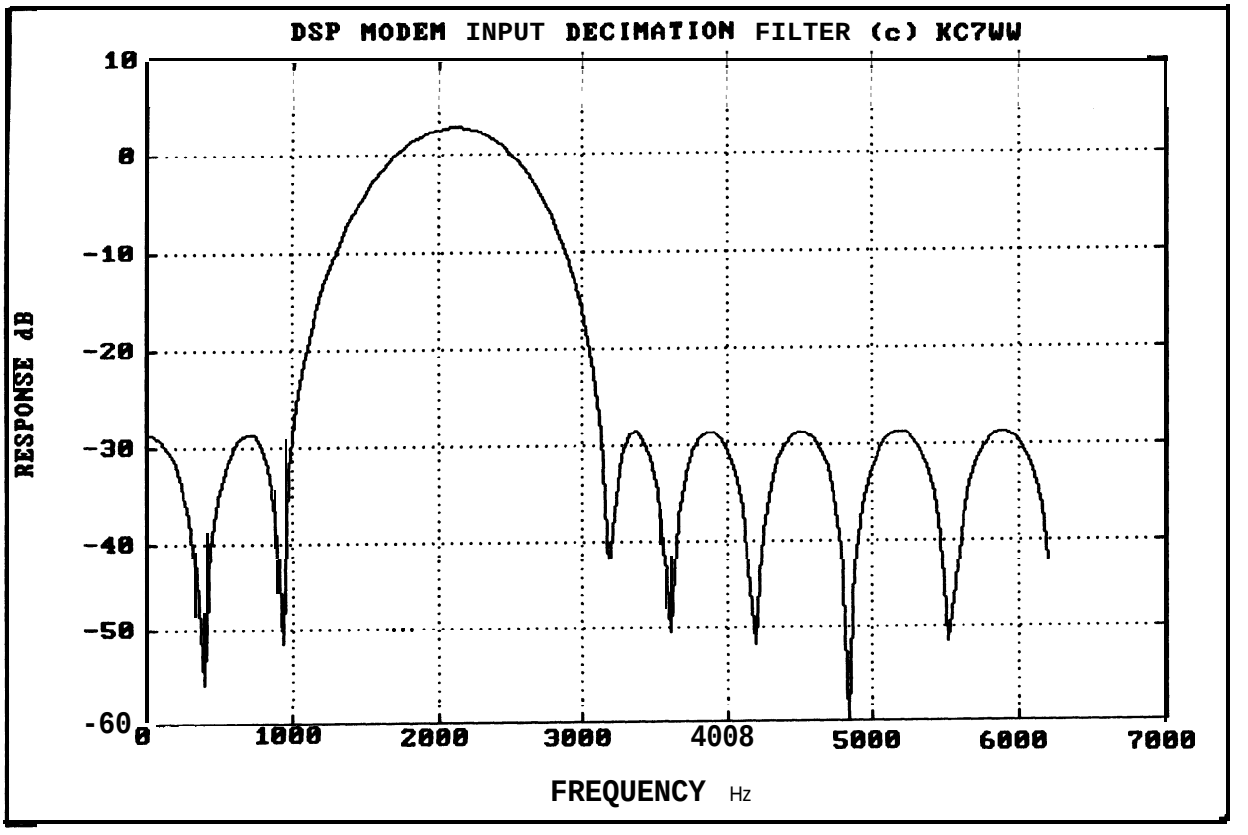
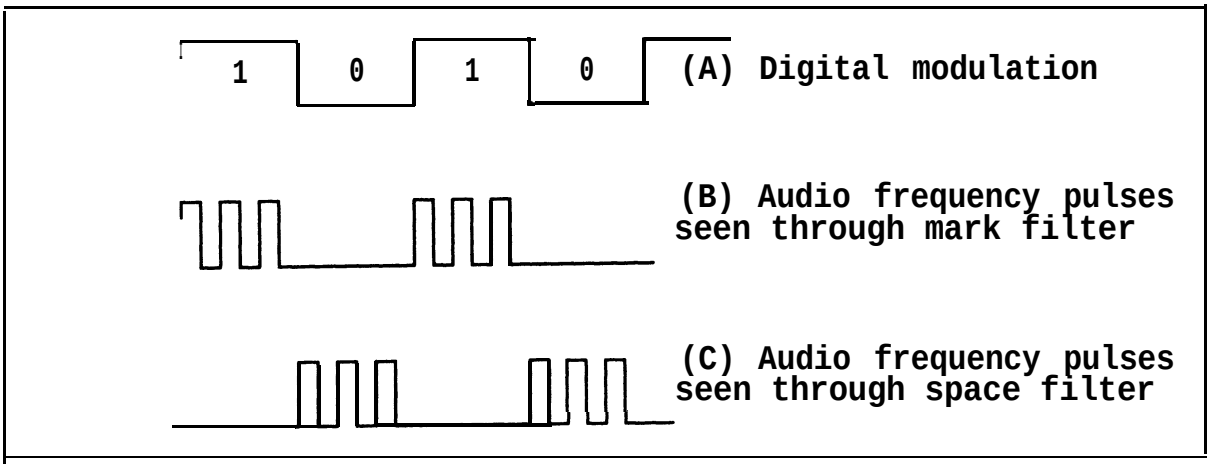


Figure 4. Input decimator filter. Note a bandpass filter is employed instead of the usual lowpass filter. Input sampling rate is 12500 Hz, output rate is 6250 Hz.



Fiqure 5. Summary of signals at various places in the discriminator. (A) The digital modulation, (B) mark, (C) space.

Matched-filter discriminator

A matched filter is simply the inverse of the impulse response of the wanted signal. Consider an input train of alternating zeroes and one's (Figure 5 (A)) where each bit time represents one signalling element, i.e. a baud. Then for 100 **baud rate,** each signalling element duration would be **1/100** th second. A signal period as seen by each filter, though would be twice this duration, or only 50 Hz as shown in Figure 5 (B) and (C). The matched filter should thus only respond to these tone pulses that has a repetition rate of 50 Hz. It can be shown that such an idealized filter would require very steep skirts, i.e. nearly infinitely small band-edge transition zones. Approximating such a filter in DSP would also require an inordinately large filter order, Practical use of the demodulator relies on the ability of **a** human operator to **"tune"** to received tones. This implies that the design should include some degree of tolerance, however, too loose tolerances will degrade performance. The DSP filters used in this DSP demodulator is shown in Figure 6.

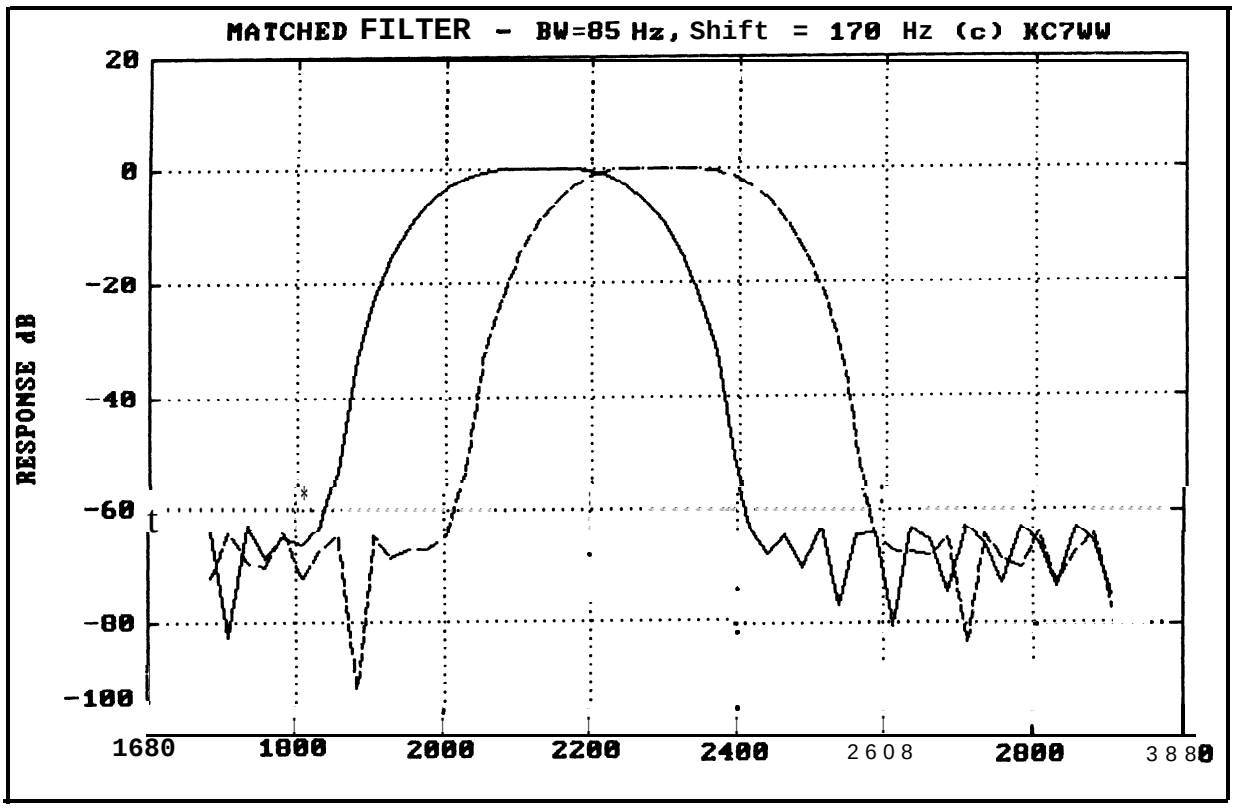


Figure 6. Matched filter pair as used for the DSP descriminator. This example shows 85 Hz wide, 81 th order FIR filters centered at 212512295 Hz. Sampling frequency is 6250 Hz. The passband of such filters are somewhat wider than an ideal matched filter to accommodate some degree of operator and equipment tolerances.

The discriminator filters as presented in Figure 6, shows minimum ripple in their passband, excellent rejection (better that 60 dB) and very steep skirts. The final function left in the discriminator, is envelope detection and signal combining. This is a rather simple task in DSP as all that is required is to take the absolute values of the discriminator signal filters and determine their difference. There still remains some audio frequency components in this difference signal, the removal of which is the subject of the next section.

Post-Uescriminator processing

The highest audio tone of interest is 2295 Hz, while the recovered modulation frequency is only 50 Hz. It is thus obvious that a simple low pass filter may be used to remove the unwanted

audio frequencies. If a cutoff frequency around 50 Hz is as well as sharp rolloff characteristics, then only the 50 Hz modulation will pass, however, the intended square-wave modulation signal will be degraded to a signal with heavily rounded edges. Some applications, such as RTTY, such slightly distorted waveforms is adequate as asynchronous character transmission is employed and it is relatively easy to estimate the center of each bit. In other instances, i.e. AMTOR and PacTOR, bit transitions are used for purposes such as bit phasing and the ability for accurately locating the bit transitions will influence the overall performance of such systems. For this reason and low pass filter with a gentle rolloff characteristic is more suitable.

There is a further consideration for the low pass filter design. At the sample rate of 6250, the output of the low pass filter would be updated every 160 microseconds. This translates to a small amount of uncertainty to where the exact bit transition occurs. As it turns out, a 6250 Hz sample rate DSP low pass filter with a cutoff frequency of 50 Hz, would require a relatively high filter order but if the sample rate could be reduced, a lower order filter with better characteristics could be designed. This DSP demodulator uses every other sample from the descriminator, i.e. reducing the sample rate to 3125 Hz before the actual low pass filter. This arrangement is effectively is also a decimator, and like in the case for the input decimator, has some desirable features that will improve overall performance. The low pass filter response is shown in Figure 7. Note that this is a very gentle low--pass filter that have been found to be adequate for most applications,i.e. RTTY, AMTOR, PacTOR, and HF Packet.

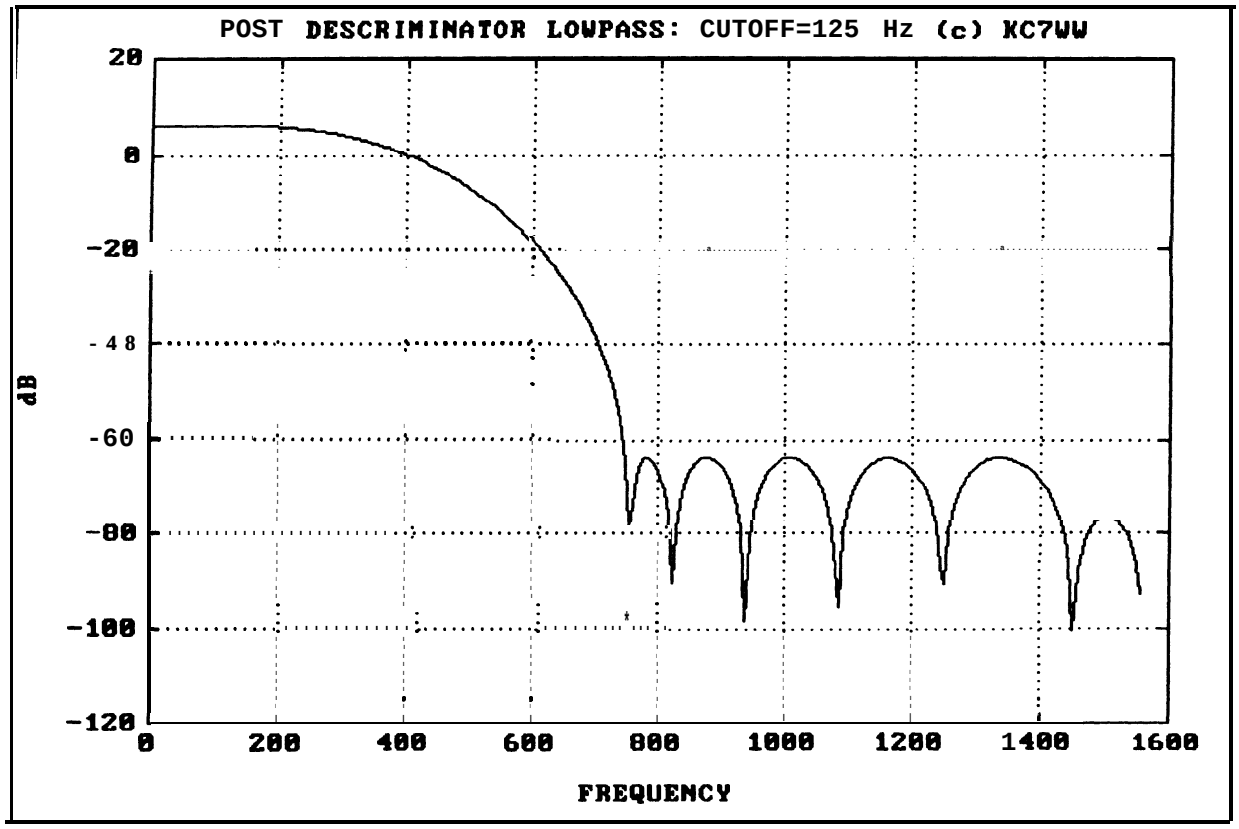


Figure 7. Post discriminator low pass filter. Cutoff, 150 Hz, filter order 15.

PERFORMANCE COMPARISONS

Performance testing and quantitive modem comparison is indeed a very difficult task. Engineering mathematicians often derive so-called "likelihood" (so-called BER) functions to estimate probable error rates in the presence of disturbances. However, this assumes that one can model the interaction of a multitude of variables such as modem architecture (whether it has a limiter or not) as well as the nature of noise on the different HF bands. This has proven to elude even the most basic of questions. What has been done successfully, however, is the application of specialized electronic atmospheric simulators. These "black boxes" is used to compare different demodulators under similar simulated "band" conditions. The DSP demodulator described in this article has not yet been tested using such sophisticated equipment, however, extensive testing against a high performance analog modem (please see AN-93 modem listed in bibliography). Under good conditions, no discernable difference could be found,

however under very adverse conditions the DSP demodulator has been found to be as good, perhaps marginally better.

SUMMARY AN CONCLUSIONS

A low cost DSP based modem for HF digital experiments have been described. It was shown that nearly ideal filters could be implemented in DSP with relative ease. Besides the added cost/performance benefits offered by a DSP approach, implementation of different modems is just a matter of downloading new code to the DSP. This flexibility implies that optimal modems for each application is readily available, something that is nearly impossible to achieve with an analog counterpart.

The author wishes to acknowledge that this article is based on the works of many gifted individuals without whose generous contributions this would not have been possible. A short bibliography is provided for further reference.

A source listing for the DSP modem, including a schematic for interfacing the DSK to an HF transceiver is available on the ADRS bulletin board for downloading as file HFDSP.ZIP

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