Digital Amateur TeleVision (D-ATV)

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August 7, 2001

Abstract

In this article, we present a Digital Amateur TeleVision (D-ATV) transmission system. Its signal can be received by cheap set-top boxes available for approximately US$100. It offers a wide user-selectable trade-off between signal bandwidth and picture quality, and at 4.5 MHz −40 dB bandwidth achieves better picture quality than analog systems.

1 Introduction

Analog Amateur TeleVision (ATV) has been in service virtually unchanged for over 20 years. Now, the industry is rapidly moving to all digital systems. Therefore, the time has come also for Amateur TeleVision to move to digital systems.

In central Europe, a significant amount of spectrum has been reserved for Digital Amateur TeleVision (D-ATV) for a number of years already, but not much has happened so far. Therefore, we decided at the Packet Radio Conference in Darmstadt, Germany, April 2001 to build a system to be shown at the Friedrichshafen Convention in June 2001.

It is clear that a complex system like a digital TV system cannot be developed from scratch as a spare time project of by small group of people in such a short time. Therefore, we wanted to use as many commercially available modules as reasonably possible.

The most widely used digital TV system is called Digital Video Broadcasting (DVB) and is based on a family of standards pioneered by the European Telecommunications Standards Institute [3]. At its core is the MPEG2 audio and video compression standard [5]. ETSI further defined three different physical layers to accommodate different transmission media.

DVB-C DVB-Cable [7] has been designed for cable networks. It uses quadrature amplitude modulation (QAM) with large constellations. It requires highly linear transmitter and receiver amplifiers and is thus unsuited to the Amateur Radio environment.

DVB-S DVB-Satellite [6] was designed for the satellite channel and uses quadrature phase shift keying (QPSK). Being designed for nonlinear traveling wave tube (TWT) amplifiers, it has benign linearity

requirements. Power amplifiers can thus be built as Amateur Radio projects with reasonable complexity. Amateur TV enthusiasts tend to use directional antennas, which greatly reduce multipath propagation.

DVB-T DVB-Terrestrial [8] has been designed for the mobile terrestrial channel with heavy multipath propagation. It uses orthogonal frequency division multiplex (OFDM). Multiple or all transmitters of the same network may share a single frequency. Unfortunately, DVB-T requires complex baseband signal processing, and furthermore DVB-T set top boxes are still scarce.

We chose DVB-S, because a huge variety of set top boxes (satellite receivers) are available on the market, and their input range ($\approx 900MHz - 2GHz$) includes the 23cm amateur radio band. The receiver chain is simple to build. It consists of DVB satellite receiver, a mixer for bands other than 23cm, an antenna and a standard TV set. The transmit chain looks different. TV studio equipment can certainly be bought, but at a price tag that is well outside of what the typical experimenter can or want to spend. So it made sense to build our own transmit chain.

2 The D-ATV Transmitter

Figure 1 depicts a block diagram of the transmit chain. A standard analog video source such as a video camera sends the signal to the MPEG2 encoder. The MPEG2 encoder converts the signal into a digital format, compresses it and sends a MPEG transport stream multiplex data stream to the baseband processor. The baseband processor performs coding and modulation tasks and produces a baseband IQ signal. The up converter converts the baseband signal to the desired carrier frequency, which is then amplified by the PA and radiated at the antenna.

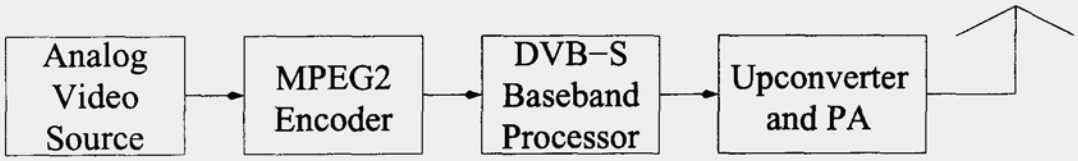

Figure 1: Block Diagram

2.1 The MPEG2 Encoder

Several companies are offering highly integrated MPEG2 encoder solutions. We chose the Fujitsu single chip MPEG-2 System Encoder LSI MB86390. An evaluation board from SR Systems [4] served our needs. Figure 2 shows the evaluation board.

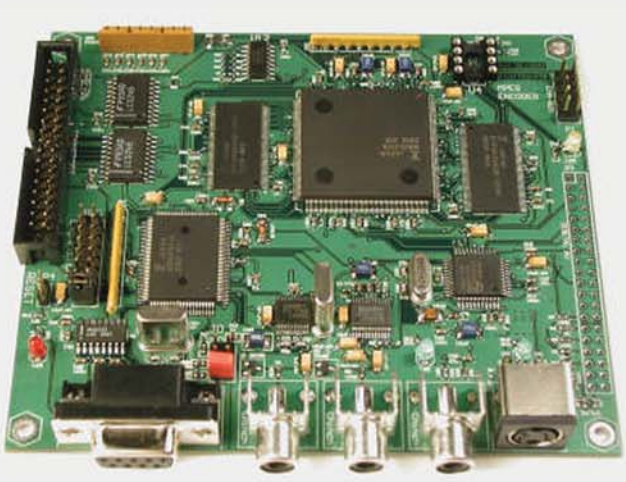

Figure 2: The Fujitsu MPEG2 Encoder Evaluation Board

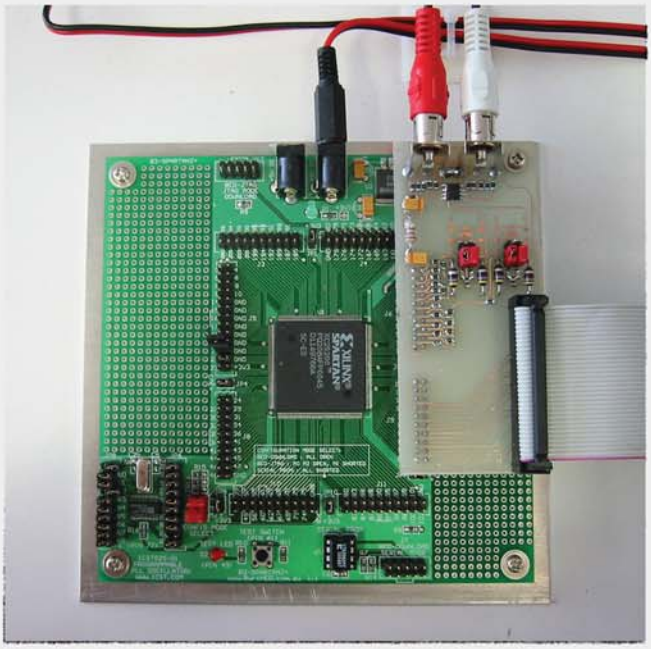

Figure 3: The Baseband Processor FPGA Board with D/A Converter Daughter Board

2.2 The Baseband Processor

Figure 4 depicts the functions performed by the DVB-S Baseband Processor. The first row of blocks operate on bytes, while the lower two blocks operate on bits.

First, the signal source, either the external MPEG2 encoder or the internal Test Data Source is selected by a jumper. The Test Data Source helped integration.

The Framing block extracts framing signals from the transport data stream and synchronizes the other modem blocks.

The Pseudo-Random Byte Sequence (PRBS) generator scrambles the data stream with a pseudo-random signal to ensure an adequate number of transitions in the signal.

The outer error correction encoder uses a Reed Solomon RS(255,239,8) code shortened to RS(204,188,8). The RS encoder operates in GF(2^8), that is on bytes. It takes an input block of 188 bytes (a MPEG2 transport stream packet) and adds 16 redundant bytes that help the receiver correct transmission errors.

The interleaver reorders the data stream. Its main purpose is to spread burst errors over multiple code words (that is 204 byte Reed-Solomon blocks).

The Parallel to Serial block converts the byte stream into a bit stream, which is then fed to the inner encoder, a Convolutional Encoder. The Convolutional Encoder produces two bits for every input bit.

Puncturing can then be used to throw away some of the generated redundant bits. The overall code rate is selectable by jumpers to be $\frac{1}{2}$, $\frac{2}{3}$, $\frac{3}{4}$, $\frac{5}{6}$ or $\frac{7}{8}$, to accommodate different data rate and error resilience needs.

The QPSK Signal Mapper then generates the QPSK signal from the Puncturing output and feeds it into two 4 times oversampling Raised-Cosine filters.

The whole Baseband Processor was implemented in a Xilinx Spartan2 XC2S200 device. We used the B3-SPARTAN2+ FPGA Board from Burch Electronic Design [1]. The device is about 10% full and achieves more than 80 MHz clock rate. This results in a symbol rate of up to 20 MSymbols/s. Figure 3 depicts the FPGA Board together with the D/A Converter Daughter Board.

We plan to increase the maximum symbol rate in the future. The current design has two speed bottlenecks. The oversampling filters may be sped up by changing the architecture. The Reed-Solomon encoder takes 16 clock cycles to encode a single byte, because it uses only one Galois Field Multiply Accumulate (GFMAC) unit. It can trivially be accelerated by using multiple GFMAC units.

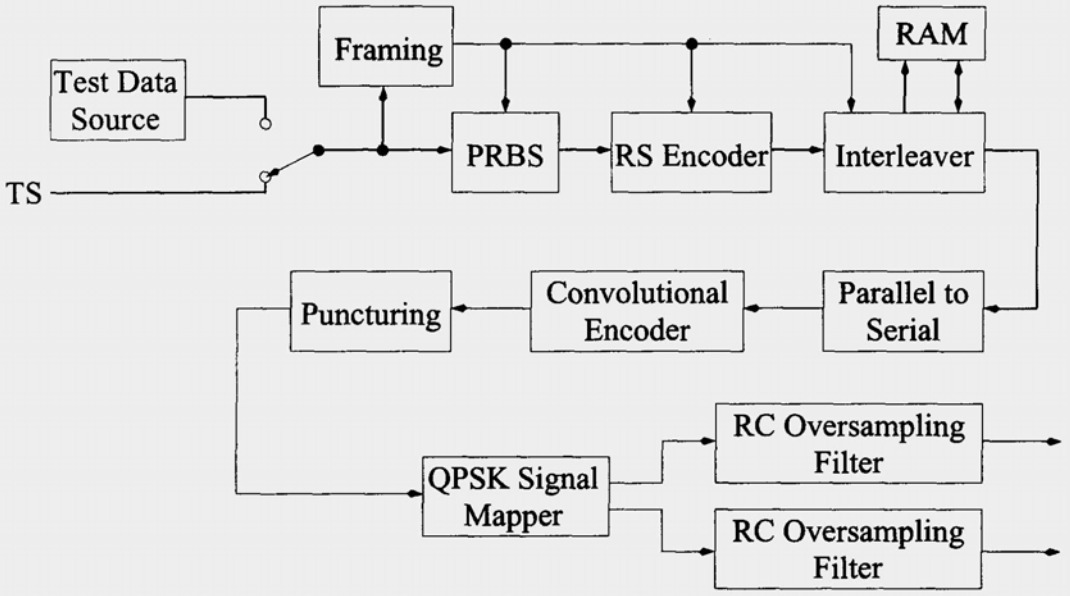

Figure 4: The DVB-S Baseband Processor

2.3 The Up Converter and PA

The QPSK RF transmitter can be realized either as a superheterodyne or as a direct transmitter. The superheterodyne concept usually achieves better carrier and sideband suppression because the operating frequency of the modulator is lower (typically below 100 MHz). But for QPSK the performance of modern integrated IQ modulators is sufficient even at 2.4 GHz; therefore a direct transmitter has been chosen which does not need bandpass filters and has thus less components and no tuning elements.

To simplify the modulator design we use ICs with integrated 90° phase shifter. Examples are RF2422 (RFMD, 0.8-2.5 GHz), AD8346 (Analog Devices, 0.8-2.5 GHz), PMB2201 (Infineon, 0.8-1.5 GHz) or MAX2721 (Maxim, 2.1-2.5 GHz). The RF2422 has been selected due to its wide bandwidth and easy availability. We also tested the MAX2721 for 2.4 GHz but had severe problems with instability[1]. The RF2422 worked very well, with some 30...35 dB carrier and side band suppression, but it is sensitive to negative spikes on the modulation inputs. After replacing it twice (and repairing some of the traces) we found the problem and added the clamping diodes in the circuit diagram. The AD8346 is considered for future trials.

The oscillator uses a MAX2620 VCO with some SMD components for the tank circuit. It is tunable between 1200 and 1300 MHz with 0-5 V tuning voltage. A slightly stronger coupling of the varicap may be useful for some extra tuning range. The LM2331 PLL (National) has been selected because it was available; in fact, most 2 GHz PLL circuits will do the job. A 2.4 GHz version of the transmitter is under development; it uses a MAX2753 fully integrated VCO and a LM2330 PLL. A PIC16F84 programs the PLL in 250 kHz steps. The loop bandwidth is about 1 kHz.

Sufficient isolation between modulator and VCO is crucial for low VCO pushing and thus low modulation distortion. Although the MAX2620 has a built-in buffer with about 35 dB isolation we added an attenuator and an extra INA340 (Agilent). For the same reason a shielding plate covers the VCO circuit and screens it from radiation from the output amplifier. The whole circuit is placed in a tin-plate box with feedthrough capacitor for the supply voltage and lowpass filters (consisting of ferrite beads and small capacitors on the backside of the PCB) on the modulation inputs. In this configuration the box can be operated close to the transmit antenna. Figure 5 depicts the IQ modulator and VCO module.

The output amplifiers uses wide band MMICs with strong internal feedback – not because they are so easy to use [2], but because the feedback improves their linearity. The output stage NGA-489 (Stanford Microdevices) has an extraordinary high IP3 = +39 dBm with only +17.5 dBm 1-dB-compression and 80 mA @ 5 V supply. At +13 dBm (20 mW) average output power or about +18 dBm PEP an ACPR (adjacent channel power rejection) of 50 dB is achievable.

The circuit is realized on a ordinary two layer FR4 board with a ground plane at the back side.

The PA should just amplify the signal without adding too much distortion. It depends on the ACPR requirements how difficult this task will be. If 40 dB or more is necessary – imagine an ATV repeater with omnidirectional antenna in the vicinity of other services in the same band – either a well-designed class AB amplifier with optimized linear 24 V transistors has to be used, or a class A amplifier. For our demonstrator we modified a M57762 (Mitsubishi) 'brick' by removing the internal bias diodes and adding external active bias circuits to each of the three stages. Operated at 4 A @ 13 V bias with a large heat sink it delivers 3 W (average) output power with only 10 mW drive and 40 dB ACPR. Figure 6 shows the output spectrum of the PA.

Instead, a class AB linear amplifier of 'SSB quality' (about 20...25 dB IM rejection) can be used followed by a bandpass filter to clean-up the spectrum. This filter can be realized in aluminium as a comb line or interdigital line resonator structure for a bandwidth of abt. 10 MHz if 1...2 dB insertion loss and

[1] The Maxim EV kit uses a 4 layer board and blocking capacitors of 0402 size

[2] In fact, the amplifier chain was oscillating at 10 GHz during the first tune-up of the circuit

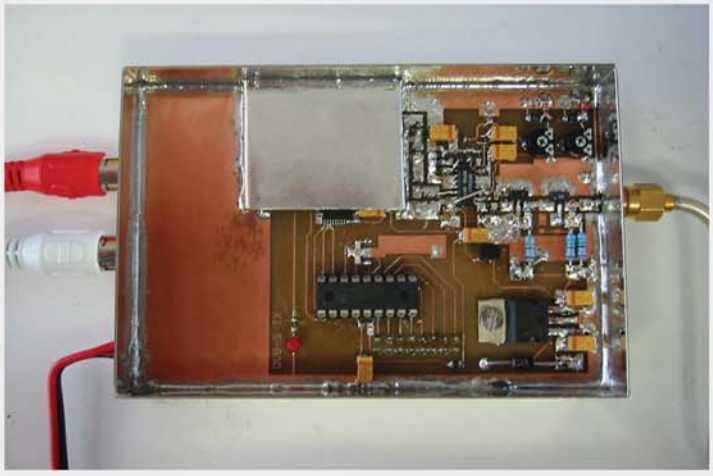

Figure 5: The IQ-Modulator and VCO Module

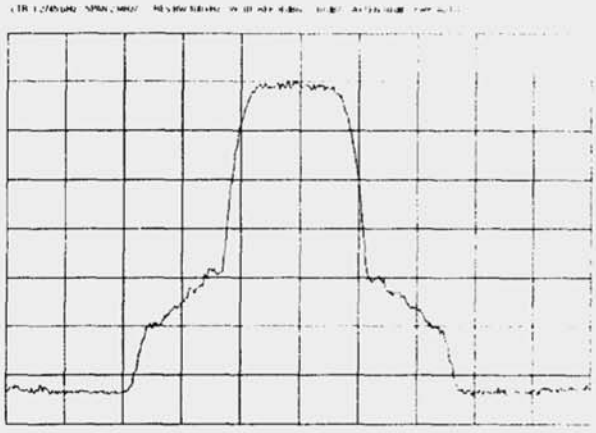

Figure 6: The Power Amplifier Output Spectrum

a careful tuning for minimum group delay distortion are accepted. For smaller bandwidths (low symbol rates), designing such a filter with low insertion loss and good thermal stability is more challenging.

For higher microwave bands, e. g. at 10 GHz, these spectral issues are usually less important for radio amateurs so that amplifiers of only moderate linearity can be used too. A transmitter can be built by up-converting a 1 or 2 GHz modulated signal; but a 10 GHz direct IQ modulator with a tuned 30 dB carrier suppression has also been published already [9].

3 Conclusion & Outlook

In this article, we presented a Digital Amateur TeleVision (D-ATV) system. The system consists of a commercially available set top box and a custom transmit chain. Using state of the art components, we were able to complete the transmit chain as a spare time project in only two months.

Figure 7 depicts DVB-S transmitter system we demonstrated at the Friedrichshafen Ham Fair in June 2001 [2]. Table 3 lists the parameters used for the demonstration. Several cheap satellite TV receivers distributed throughout the fair hall received the signal.

Given sufficient interest, Stefan Reimann, DG8FAC plans to produce a small quantity of the transmit chain boards.

Since the Xilinx FPGA device is now only about 10% full, there are numerous extensions possible, such as

- multiplexing several sources onto the same carrier
- increasing the maximum symbol rate of the Baseband Processor
- filling unused MPEG2 transport frames with network data, such as AX.25 or TCP/IP traffic

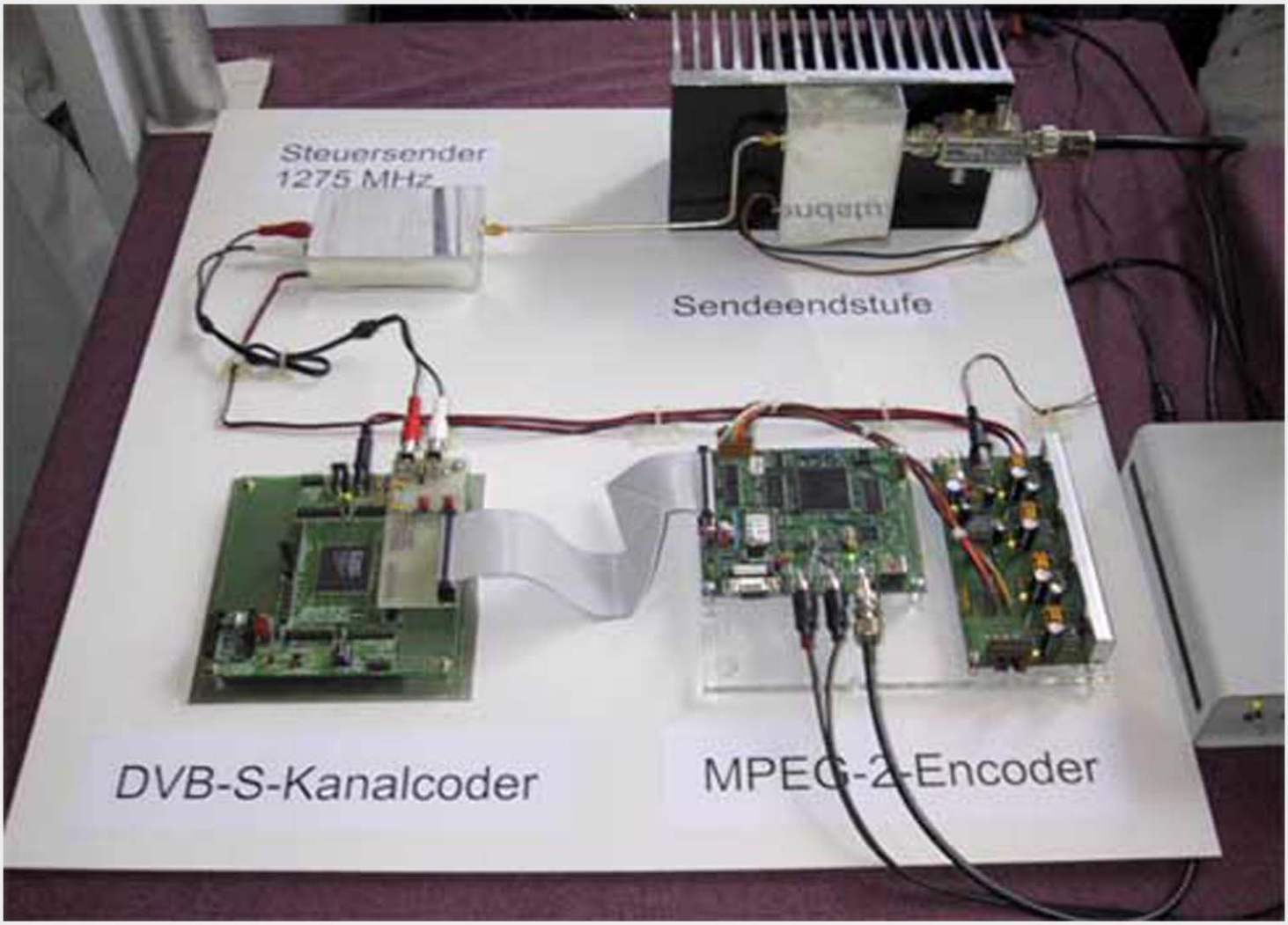

Figure 7: The Complete DVB-S Transmitter demonstrated at the Friedrichshafen Ham Fair

Transmit Frequency	1275 MHz
Symbol Rate	3 MSymbols/s
Bandwidth	4 MHz
Convolutional Code Rate	$\frac{5}{6}$
MPEG2	MP@ML D1 4:3
	25 Frames/s
	4.5 MBit/s
Transmit Power	2 Watts
Antenna	vertically polarized, omnidirectional

Table 1: Friedrichshafen Demonstration Parameters

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